TOSHIBA CMOS Digital Integrated Circuit Silicon Monolithic

TC90A92AFG

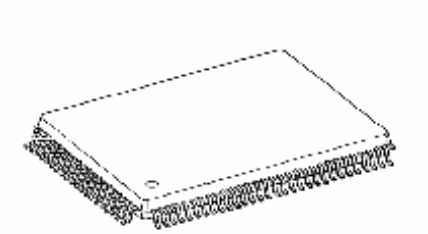
3D comb & Video Decoder

TC90A92AFG is a 1chip LSI of 3 dimensional Y/C separation and color decoder.

TC90A92AFG has 10bit A/D converter and 8bit A/D converter for analog Video signal and 1H component signal.

and it also has 4Mbit DRAM for NTSC 3D comb. In case of PAL system, 3 line comb is available.

The internal color decoder is adaptive to multi color system.



QFP100-P-1420-0.65Q

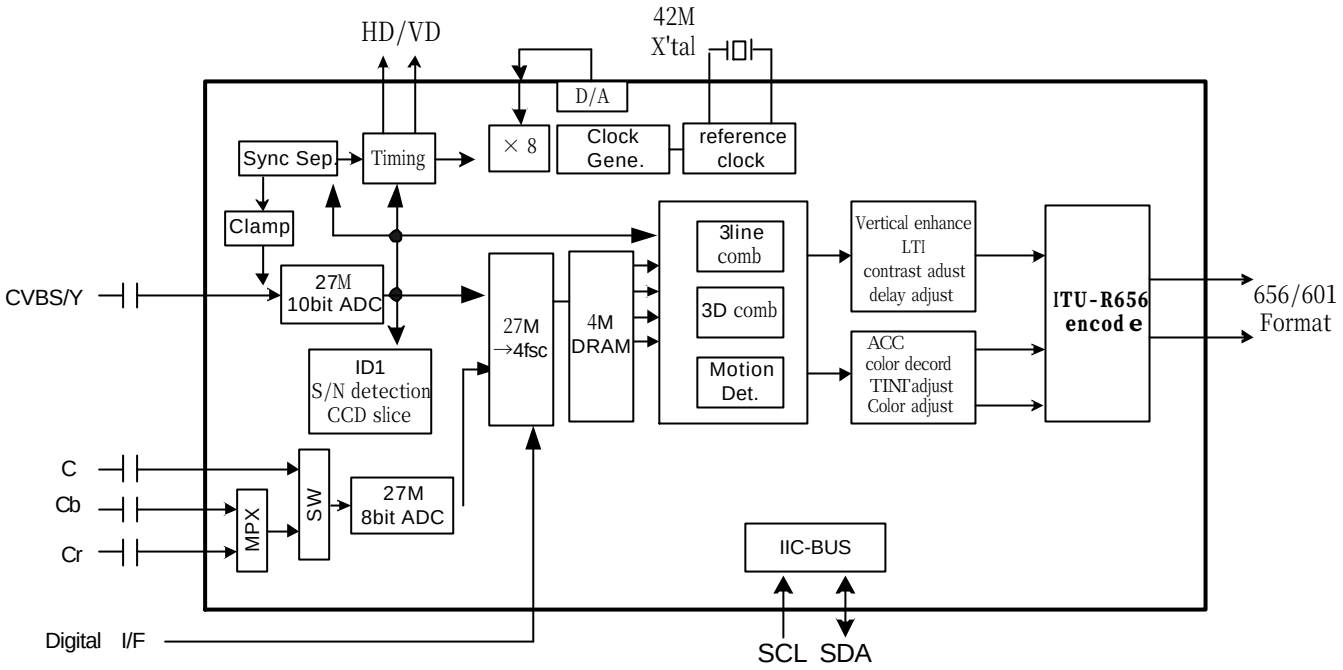
Mass : 1.6g (TYP)

Feature

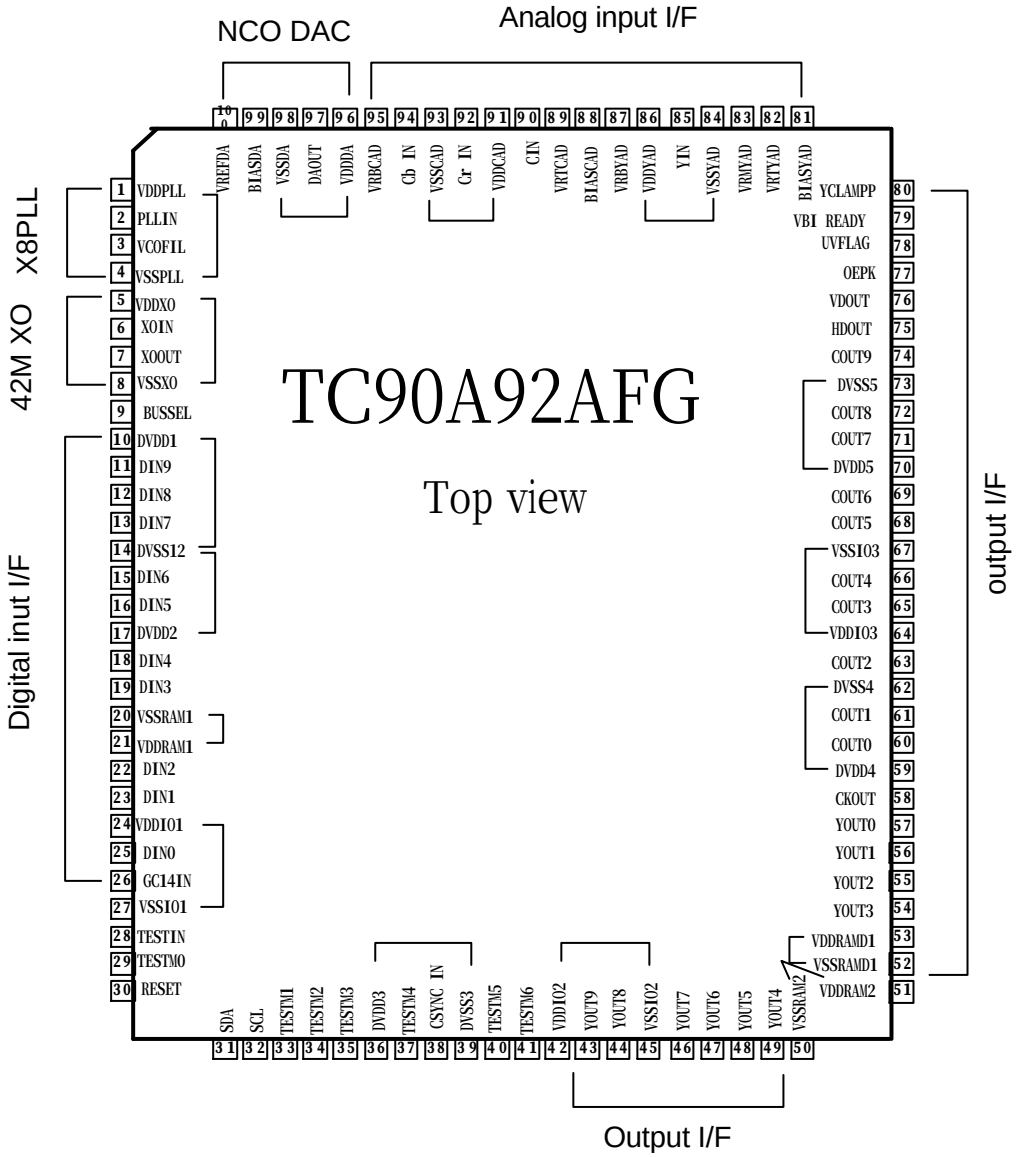
- Multi color system
- Input I/F : CVBS / S / YCbCr
- 3DYCS : NTSC system
- 3lineYCS+3D YNR/CNR : Multi color system
  (SECAM : BPF YCS)
- Output I/F : 656 / 601
- Picture improvement
  Y : Vertical enhance / LTI / Contrast / Set up adjust
  C : TOF / ACC / Color decode /
  Color gain /CTI / offset adjust
- S/N detection / ID1 data slice / CCD data slice
- I^2C bus control
- Package : QFP 100
- Power supply : 1.5V, 2.5V, 3.3 V

Version 1.5

1. Block diagram



2. Pin layout



3. Terminal description

Pin No.	Pin Name	Function	Durable voltage (V)	I/O	Circuit System (Analog or Digtal)	DC of standard operation (V)	Analog signal effective level (Vp-p)
1	VDDPLL	Power supply for X8 PLL circuit	2.5	VDD	Analog	2.5	-
2	PLLIN	Input terminal of X8 PLL circuit	2.5	IN	Analog	1.25	0.5～VDDPLL*0.8
3	VCOFIL	Filter terminal for X8 PLL circuit	2.5	Bypass	Analog	1.2	-
4	VSSPLL	GND for X8 PLL circuit	0	GND	Analog	0	-
5	VDDXO	Power supply for X' tal OSC circuit	3.3	VDD	Digital	3.3	-
6	XOIN	X' tal OSC circuit input terminal	3.3	IN	Digital	-	-
7	XOOUT	X' tal OSC circuit output terminal	3.3	OUT	Digital	-	-
8	VSSXO	GND for X' tal OSC circuit	0	GND	Digital	0	-
9	BUSSEL	Select IIC slave address (L :B0 Hi :B2)	3.3	IN	Digital	-	-
10	DVDD1	Power supply for Logic circuit	1.5	VDD	Digital	1.5	-
11	DIN9	Composite video signal digital input terminal (MSB) (DIN0～DIN9 : input terminal for GR) (In case not use :DIN0-9 are connected to GND)	3.3	IN	Digital	-	-
12	DIN8	Composite video signal digital input terminal	3.3	IN	Digital	-	-
13	DIN7		3.3	IN	Digital	-	-
14	DVSS12	GND for Logic circuit	0	GND	Digital	0	-
15	DIN6	Composite video signal digital input terminal	3.3	IN	Digital	-	-
16	DIN5		3.3	IN	Digital	-	-
17	DVDD2	Power supply for Logic circuit	1.5	VDD	Digital	1.5	-
18	DIN4	Composite video signal digital input terminal	3.3	IN	Digital	-	-
19	DIN3		3.3	IN	Digital	-	-
20	VSSRAM1	GND for internal DRAM	0	GNG	Digital	0	-
21	VDDRAM1	Power supply for internal DRAM	1.5	VDD	Digital	1.5	-
22	DIN2	Composite video signal digital input terminal	3.3	IN	Digital	-	-
23	DIN1		3.3	IN	Digital	-	-
24	VDDIO1	Power supply for I/O	3.3	VDD	Digital	3.3	-
25	DIN0	Composite video signal digital input terminal	3.3	IN	Digital	-	-
26	GC14IN	External 4fsc clock input terminal for Using DIN0-9 terminal (In case not use : connect to GND)	3.3	IN	Digital	-	-
27	VSSIO1	GND for I/O	0	GND	Digital	0	-
28	TESTIN	Clock terminal for Test mode	3.3	IN	Digital	0	-
29	TESTM0	Terminal for Test mode	3.3	IN	Digital	0	-
30	RESET	Reset terminal (Low :Reset Hi :normal)	3.3	IN	Digital	3.3	-
31	SDA	IIC SDA terminal (5V input possible)	5	I/O	Digital	-	-
32	SCL	IIC SCL terminal (5V input possible)	5	IN	Digital	-	-
33	TESTM1	Terminal for Test mode	3.3	IN	Digital	0	-
34	TESTM2		3.3	IN	Digital	0	-
35	TESTM3		3.3	IN	Digital	0	-
36	DVDD3	Power supply for Logic circuit	1.5	VDD	Digital	1.5	-
37	TESTM4	Terminal for Test mode	3.3	IN	Digital	0	-
38	CSYNCIN	External composite Sync signal input	5	IN	Digital	0	-
39	DVSS3	GND for Logic circuit	0	GND	Digital	0	-
40	TESTM5	Terminal for Test mode	3.3	IN	Digital	0	-
41	TESTM6		3.3	IN	Digital	0	-
42	VDDIO2	Power supply for I/O	3.3	VDD	Digital	3.3	-
43	YOUT9	Digital video port output (MSB) 656/ 601 8bit mode :YCbCr 601 :Y)	3.3	OUT	Digital	-	-
44	YOUT8	Digital video port output8	3.3	OUT	Digital	-	-
45	VSSIO2	GND for I/O	0	GND	Digital	0	-
46	YOUT7	Digital video port output7	3.3	OUT	Digital	-	-
47	YOUT6	Digital video port output6	3.3	OUT	Digital	-	-
48	YOUT5	Digital video port output5	3.3	OUT	Digital	-	-
49	YOUT4	Digital video port output4	3.3	OUT	Digital	-	-
50	VSSRAM2	GND for internal DRAM	0	GND	Digital	0	-

Pin No.	Pin Name	Function	Durable voltage (V)	I/O	Circuit System (Analog or Digtal)	DC of standard operation (V)	Analog signal effective level (Vp-p)
51	VDDRAM2	Power supply for internal DRAM	1.5	VDD	Digital	1.5	-
52	VSSRAMD1	GND for internal DRAM	0	GND	Digital	0	-
53	VDDRAMD1	Power supply for internal DRAM	2.5	VDD	Digital	2.5	-
54	YOUT3	Digital video port output	3.3	OUT	Digital	-	-
55	YOUT2		3.3	OUT	Digital	-	-
56	YOUT1	Digital video port output (In case 8bit output mode : fixed to Low)	3.3	OUT	Digital	-	-
57	YOUT0		3.3	OUT	Digital	-	-
58	CKOUT	System Clock output terminal for digital video signal output 656 : 27MHz 601 : 13.5MHz	3.3	OUT	Digital	-	-
59	DVDD4	Power supply for Logic circuit	1.5	VDD	Digital	1.5	-
60	COUT0	Cb/Cr digital video signal output (LSB) 656 : fixed Low 601 : Cb/Cr) (In case 16bit mode: LSB and 2'nd LSB are fixed Low)	3.3	OUT	Digital	-	-
61	COUT1		3.3	OUT	Digital	-	-
62	DVSS4	GND for Logic circuit	0	GND	Digital	0	-
63	COUT2	Cb/Cr digital video signal output	3.3	OUT	Digital	-	-
64	VDDIO3	Power supply for I/O	3.3	VDD	Digital	3.3	-
65	COUT3	Cb/Cr digital video signal output	3.3	OUT	Digital	-	-
66	COUT4		3.3	OUT	Digital	-	-
67	VSSIO3	GND for I/O	0	GND	Digital	0	-
68	COUT5	Cb/Cr digital video signal output	3.3	OUT	Digital	-	-
69	COUT6		3.3	OUT	Digital	-	-
70	DVDD5	Power supply for Logic circuit	1.5	VDD	Digital	1.5	-
71	COUT7	Cb/Cr digital video signal output	3.3	OUT	Digital	-	-
72	COUT8		3.3	OUT	Digital	-	-
73	DVSS5	GND for Logic circuit	0	GND	Digital	0	-
74	COUT9	Cb/Cr digital video signal output (MSB)	3.3	OUT	Digital	-	-
75	HDOUT	Horizontal reference timing pulse	3.3	OUT	Digital	-	-
76	VDOUT	Vertical reference timing pulse	3.3	OUT	Digital	-	-
77	OEPK	Field detection output / Pedestal pulse output	3.3	OUT	Digital	-	-
78	UVFLAG	Reference pulse of multiplexed Cb/Cr signal	3.3	OUT	Digital	-	-
79	VBIREADY	Reference pulse of IIC read for VBI data slice Function (Hi level at 23 line and 286 line)	3.3	OUT	Digital	-	-
80	YCLAMPP	Clamp signal for YIN	3.3	OUT	Digital	-	-
81	BIASYAD	The bias terminal for internal 10bit ADC	2.5	Bypass	Analog	0.8	-
82	VRTYAD	The reference top voltage terminal of internal 10bit ADC	2.5	Bypass	Analog	1.75	-
83	VRMYAD	The reference middle voltage terminal of Internal 10bit ADC	2.5	Bypass	Analog	1.25	-
84	VSSYAD	GND for internal 10bit ADC	0	GND	Analog	0	-
85	YIN	Analog CVBS/Y signal input terminal for Internal 10bit ADC	2.5	IN	Analog	-	VDDYADx0.4
86	VDDYAD	Power supply for internal 10bit ADC	2.5	VDD	Analog	2.5	-
87	VRBYAD	The reference bottom voltage terminal of Internal 10bit ADC	2.5	Bypass	Analog	0.75	-
88	BIASCAD	The bias terminal for internal 8bit ADC	2.5	Bypass	Analog	0.8	-
89	VRTCAD	The reference top voltage terminal of Internal 8bit ADC	2.5	Bypass	Analog	1.75	-
90	CIN	Analog C signal input terminal for Internal 8bit ADC	2.5	IN	Analog	1.25	VDDCADx0.4
91	VDDCAD	Power supply for internal 8bit ADC	2.5	VDD	Analog	2.5	-
92	CRIN	Analog Cr signal input terminal for Internal 8bit ADC	2.5	IN	Analog	-	VDDCADx0.4
93	VSSCAD	GND for internal 8bit ADC	0	GND	Analog	0	-
94	CBIN	Analog Cb signal input terminal for Internal 8bit ADC	2.5	IN	Analog	-	VDDCADx0.4
95	VRBCAD	The reference bottom voltage terminal of internal 8bit ADC	2.5	Bypass	Analog	0.75	-
96	VDDDA	Power supply for internal DAC of NCO	2.5	VDD	Analog	2.5	-
97	DAOUT	Output terminal of DAC of NCO	2.5	OUT	Analog	2	VDDDA-VDDDA*0.6
98	VSSDA	GND for internal DAC of NCO	0	GND	Analog	0	-
99	BIASDA	The bias terminal for internal DAC	2.5	Bypass	Analog	0.9	-
100	VREFDA	The reference voltage terminal of DAC	2.5	Bypass	Analog	1.5	-

(Note) Please the capacitor of the power supply terminal and the BIASAD terminal is placed near the terminal.

4.1 Introduction

TC90A92AFG is a signal processor for normal scan (525i, 625i) signal.

1. TC90A92AFG has input interface for CVBS, S and component video signals.
2. TC90A92AFG has a 3D YCS function for M-NTSC signal with internal 4Mbit DRAM.
   And in case of 3line YCS mode it is available to use 3D YNR & CNR function.
3. TC90A92AFG has a 3D YNR & CNR for S terminal input and 1H component signal.
4. TC90A92AFG has a digital input interface for Ghost reduction LSI.
5. TC90A92AGF has color decoder circuit for multi video system and cync separation circuit.
6. Selectable automatic color system detection mode and forced color system mode.
7. TC90A92AFG has picture quality improve function.
8. TC90A92AFG has ITUR-656 and 601 output interface.
9. TC90A92AFG has S/N detection, ID-1 data slice and CCD data slice function for M-NTSC and it is available to read via IIC read mode.

4.2 Function

(1) Input stage

The input video signal (CVBS/S / YCbCr) is converted to digital video signal by internal A/D converter of TC90A92AFG. TC90A92AFG generates the fH synchronous clock (27MHz) from the digital video signal by using

PLL circuit, H sync separation circuit and H sync regeneration circuit.

This clock is generated by internal digital VCO circuit which has 42MHz X'tal oscillation circuit as a reference clock.

(2) Input interface

a) Setting for input mode

Input signal can be set via INSEL at sub address 00 hex.

INSEL : 00: CVBS 01: S input 10: YCbCr 11: GR digital input

b) Dynamic range of the internal ADC

TC90A92AFG has a 10bit ADC for analog CVBS, Y signal of S input and Y signal of component.

For color signal (chroma & CbCr), TC90A92AFG has a another 8bit ADC.

Dynamic range of the internal ADC is designed by AVDD×0.4(Reference level : 1Vp-p).

Recommend amplitude of analog video signal input is 0.7Vp-p (140IRE).

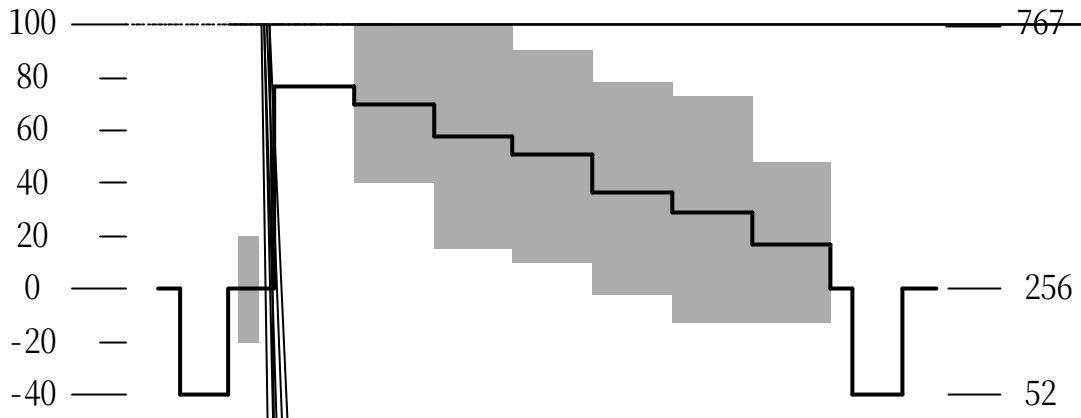


Fig-1 : YAD Input Level (Example : CVBS Input)

Fig-2 : CAD Input Level (Example : Cb Input Signal)

When using YCbCr mode, it is cautious of the input level to CAD (color system 8bit AD).
As shown in Fig-2, the standard input level of the CAD is 0.7Vp-p.

c) Clamping

The clamp control circuit controls the correct clamping of the analog input signals.
Clamp level for CVBS and Y signal is 256 LSB (10bit unit). For C and Cb/Cr are 128 LSB (8bit unit).

d) Cb /Cr input

Cb and Cr signals are multiplexed in front of internal 8bit ADC.
Offset adjustment is available independently.

TOSHIBA

Aug./2003

(4) TV system detection for CVBS and S input

TV system auto detection is set via register [AUTODET] at sub address 00 hex.

00 : forced TV mode (color system is set via [TVM] at sub address 00 hex.

It is fixed to color system which is selected by [Select FSC], [Select FV], [Select PAL], [Select SECAM].

When there is difference between selected TV system and input TV system, it can't detect fsc signal for read mode.

There is no relation to setting [Select FV] and input signal gives priority.

01 : European mode (fsc detection : 4.43MHz / 3.58MHz)

Color system is determined by result of vertical frequency detection, fsc detection, SECAM detection.

The order of priority for distinction is 4.43PAL, NTSC, SECAM, ACK.

10 : South American mode (fsc detection : 3.57954MHz /3.5756MHz /3.5820MHz)

Color system is determined by result of fsc detection, vertical frequency detection.

The order of priority for distinction is 3.58PAL, 3.58NTSC, ACK.

11 : full multi mode

Color system is determined by result of vertical frequency detection, fsc detection, SECAM detection.

The order of priority for distinction is PAL, NTSC, SECAM, ACK.

And the distinction of 50/60Hz are independently, there is no priority.

(In case of non signal, it keeps the value of last time.)

(5) Sync processing

TC90A92AFG has a H/V sync separation circuit and regenerates HD/VD pulse.

The phase of HD and VD signals are selectable. (Adapt to 656 format and synchronized with input signal phase)

(6) Y/C separation and noise reduction

TC90A92AFG has an adaptive comb filter and noise reduction circuit.

M-NTSC : Motion adaptive 3D comb (The sensitivity of motion detection for Y & C are set independently.)

Other color system (Not M-NTSC and not SECAM) : 3D YNR and CNR after 3line comb

SECAM : BPF+3D YNR. 3D CNR is simple motion (Not edge detection).

The function is shown in a table-1.

TV signal	Field Frequency	Input signal		
		CVBS	S	YCbCr
PAL	50Hz	2DYCS+3DYNR+3DCNR	3DYNR+3DCNR	—
N PAL		2DYCS or BPF+3DYNR+3DCNR	3DYNR+3DCNR	—
SECAM		BPF +3DYNR	3DYNR	—
NTSC-50		2DYCS or BPF+3DYNR+3DCNR	3DYNR+3DCNR	
Component-50		—	—	3DYNR+3DCNR
M NTSC	60Hz	3DYCS or 2DYCS+3DYNR+3DCNR	3DYNR+3DCNR	—
4.43NTSC		2DYCS or BPF+3DYNR+3DCNR	3DYNR+3DCNR	—
M PAL		2DYCS or BPF+3DYNR+3DCNR	3DYNR+3DCNR	—
PAL-60		2DYCS or BPF+3DYNR+3DCNR	3DYNR+3DCNR	—
SECAM-60		BPF +3DYNR	3DYNR	
Component-60		—	—	3DYNR+3DCNR

Table-1

Note : Field noise reduction for 625 system

(7) Take off filter (TOF)

TC90A92AFG has a take off filter in front of internal color decoder.

Characteristic of TOF is set via [TOF] at sub address 0F hex.

000 : OFF

001 : BPF for cross color reduction is active.

010 –111： type2 – type7

(8) Y process

a) Vertical enhance : available to set coring, gain and non-linear performance

b) LTI function

f0 is selectable (3.3MHz/ 2.2MHz).

Coring level is selectable (0.8IRE/ 1.6IRE/ 3.2IRE/ 6.4IRE).

Gain is selectable (OFF/ x1/8 / x1/4 / x1/2).

c) Sharpness

f0 is selectable (4.2MHz/ 3.3MHz).

Coring level is selectable (0.8IRE/ 1.6IRE/ 3.2IRE/ 6.4IRE).

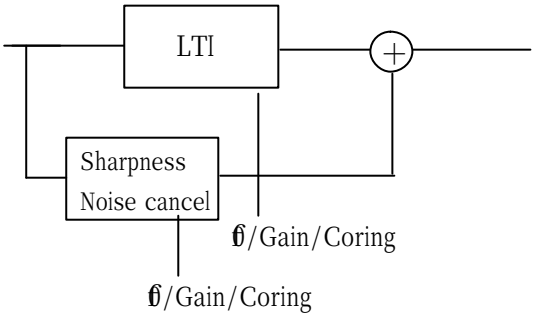
Gain is selectable (OFF/ x1/8 / x1/4 / x1/2).

d) Noise chancellor

f0 is 4.2MHz.

Gain is selectable (OFF/ x1/4 / x1/2 / x1).

Coring level is selectable (0.8IRE/ 1.6IRE/ 3.2IRE/ 6.4IRE).



e) Contrast

Control range is –6dB --- +7.6dB (The color becomes a saturation depending on input level.)

f) Brightness control

Control range is 0LSB ---+ 60LSB (10bit unit)

Brightness control is effective at the period of picture area.

(9) C process

a) ACC control : A reference level is set up by register ACC LEVEL. (Recommended value is under 3)

b) Killer control : sensitivity of killer is set via [COLOR KILL LEVEL] at sub address 0E hex.

In case Killer detection, comb filter for Y becomes off.

c) HUE control : Hue control is available for CVBS and C signal of NTSC system.

Hue bias : 0 --- +45degree

Hue range : -45 degree --- +43.6degree

Base band Tint control is available for component signal input mode.

Hue range : -45 degree --- +43.6degree

d)Sub color gain control

Amplitude of Cb and Cr signals are controlled via IIC.

Control range is –6dB --- +2.8dB

e)CTI function

f0 is selectable (1.7MHz/ 3.3MHz).

Coring level is selectable (0.4IRE/ 0.8IRE/ 1.6IRE/ 3.2IRE).

Gain is selectable (OFF/ x1/8 / x1/4 / x1/2).

f) Offset control of the period of picture area

The DC level of the Cb and Cr signals are controlled via IIC independently.

Control range : -8LSB ---- +7LSB (10bit unit)

(10) Output format

656 output mode / 601 output mode (CKOUT ：the polarity is selectable)

8bit mode /10bit mode selectable

Y ：pedestal = 16LSB (8bit unit)

C ：128LSB (8bit unit) (except the period of picture area)

It is selectable 601 or 656 format at sub address 01hex :D4 [FORMATO]

It can limit to the signal under 16LSB(in 8 bit) at sub address 23hex :D2 [CLP]

In case of standard 656 output, it is necessary to set to limit.

YOUT, COUT and CKOUT can be set Hi-Z mode via IIC.

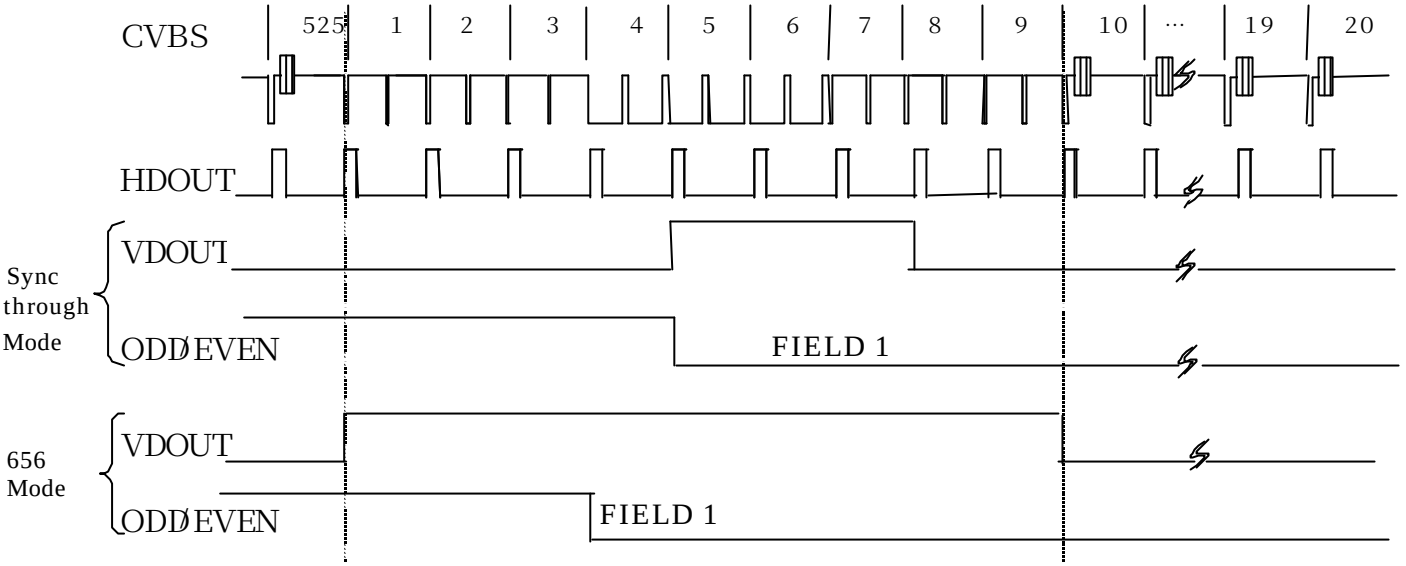
Pin	Bit	Data rate	Comment
YOUT [0-9]	8/10	13.5MHz/27MHz	601mode:Y signal 656 mode: YCbCr (CK:27MHz)
COUT [0-9]	8/10	6.75MHz	Cb/Cr (CK:13.5MHz) e38.5 415.388081 T 95 Tw ( ) Tj 121.5

.

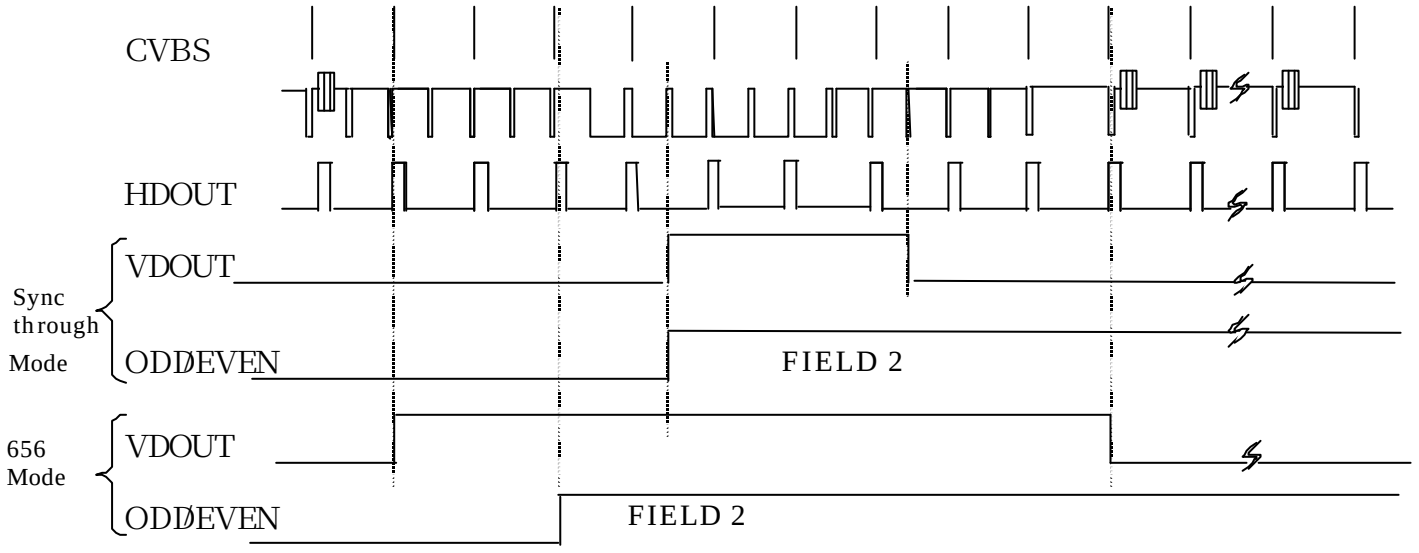
a) Vertical output timing

a-1) 525/60Hz input

(first field)

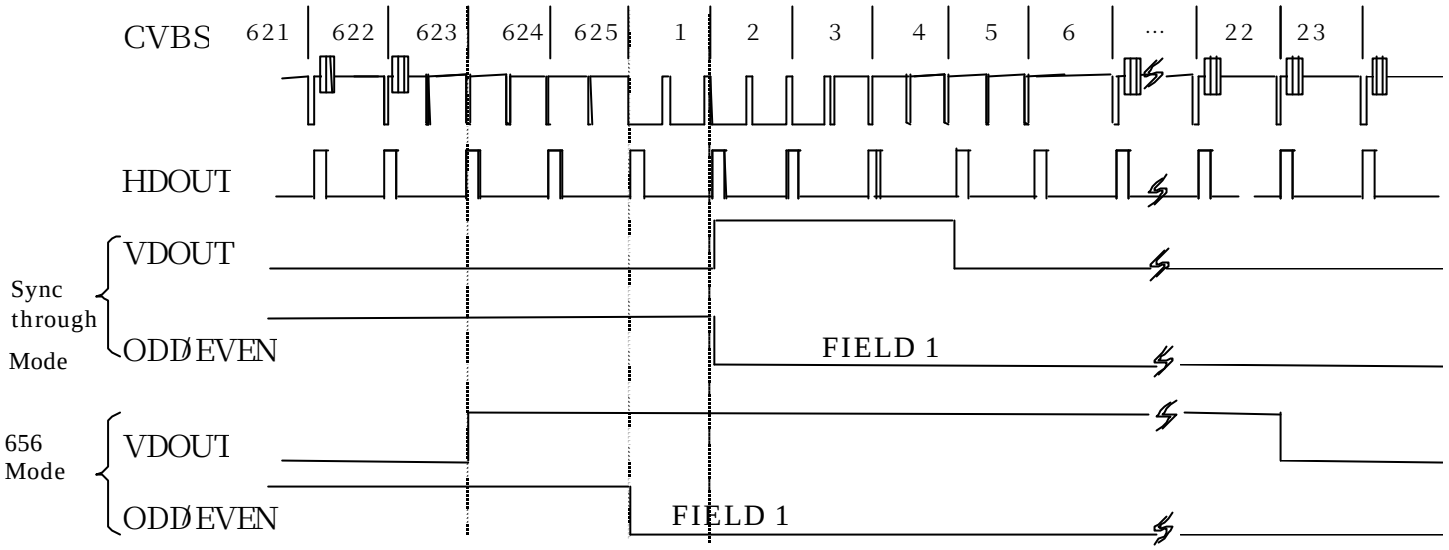


(2n'd field)

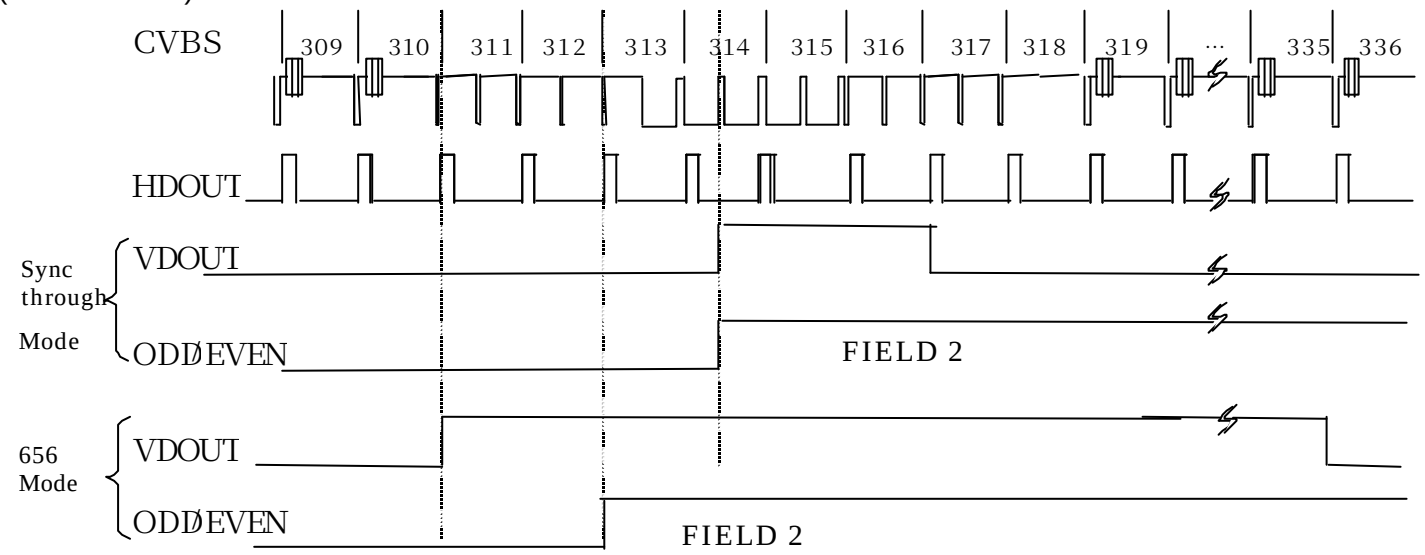


a-2) 625/50Hz input mode

(1st, 3thd field)



(2'nd 4thd field)



Width of HD and VD pulse at Sync through mode

	525	625
HD pulse	4.74us (128ck at 27MHz)	
VD pulse	3H	2.5H

Width of HD pulse at 656 format is the same as the period between EAV and SAV.

In case of input signal is non standard at 656 format, it may not be above value.

(11) Feature function

a) S/N detection

Noise detection is performed in the vertical blanking period. Detection is performed at every field and the data is updated each field. A S/N detection result is 8bit data and it can be read via IIC.

b)ID-1 data slice function

TC90A92AFG has a data slice circuit for ID-1 signal at the line 20 and 283.
Sliced data can be read via IIC.
This function is only output of sliced data level.
It is necessary to check a continuation of signal between some fields for ID-1 signal detection.

c) CCD data slice function

TC90A92AFG has a data slice circuit for closed caption data at the line 21 and 284.
CRI detection, start bit detection and sliced data can be read via IIC.
VBI READY (Pin79) is a reference timing pulse for S/N detection and VBI data slice function.
VBI READY outputs Hi pulse at the line 23 and 286.

d)Others

TC90A92AFG has IIC read registers.
50/60Hz detection/ signal detection / V sync detection / locked unlocked detection / 4.43MHz fsc detection / PAL detection / SECAM detection / Killer detection

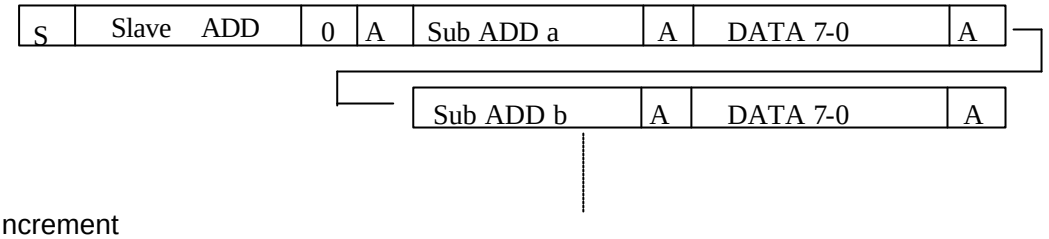
5.IIC BUS

The slave address of TC90A92AFG can use two, B0hex and B2hex. A slave address is chosen by BUS SELL of a terminal 9 (BUS SELL=L:B0hex , BUS SELL=H:B2hex).

In addition to usual transmission, a transmission format can use continuation transmission and the auto increment mode.

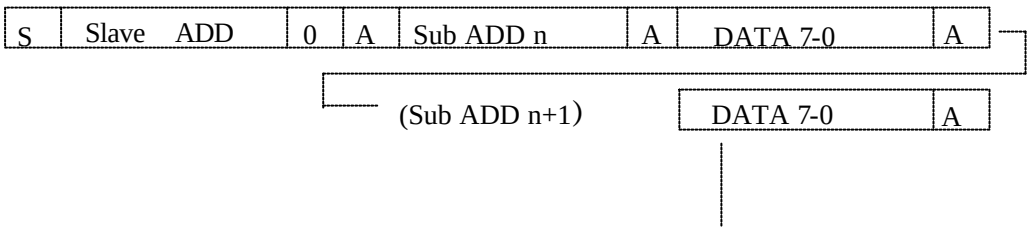
(a) Continuation transmission

（The sub-address of a register to change is specified. MSB of a sub-address is set to 0 at this time.）



(b) Auto increment

（The increment of the sub-address is carried out one by one from N. MSB of a sub-address is set to 1 at this time.）



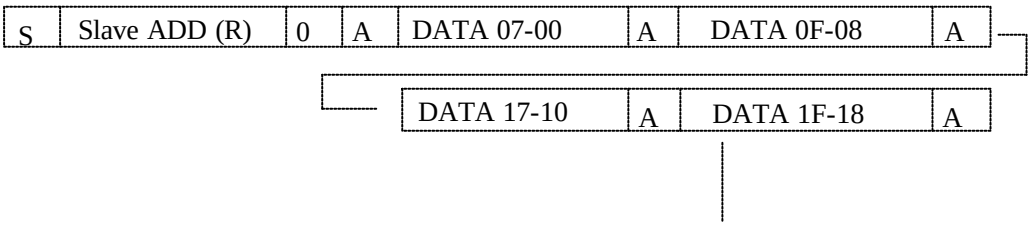
(c) IIC read

If it sets to 1 for LSB of slave address , it can read data.

It starts data output from TC90A92AFG after

TC90A92F is the master and the micro controller is slave.

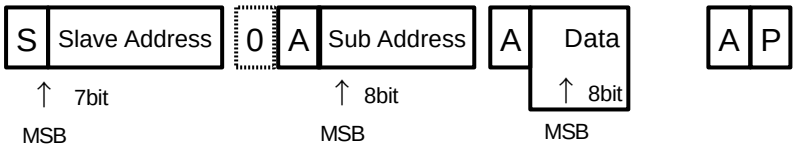
To suspend transmission, deliberately generate an acknowledge error.



I2C BUS control format outline

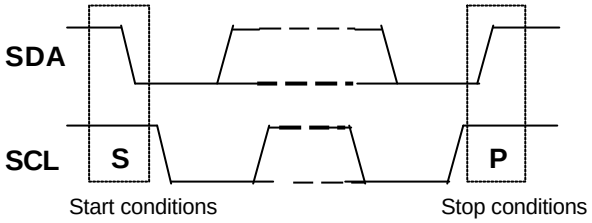
The BUS control format of TC90A92F is based on the PHILIPSI2C BUS control format.

Data transmission format

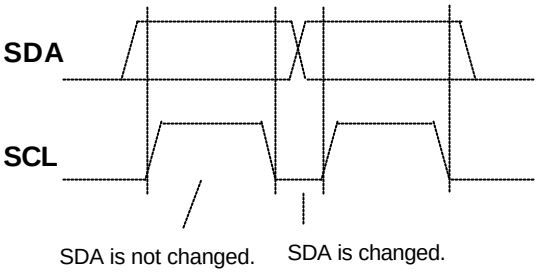


S: Start conditions
P: Stop conditions
A: Acknowledgement

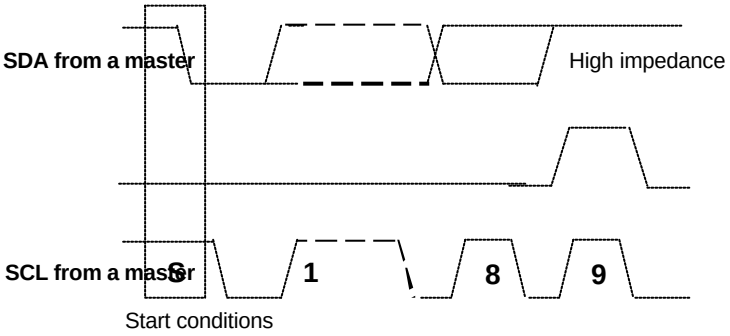
(1) Start conditions, Stop conditions



(2) Bit transmission



(3) Acknowledgement



A6	A5	A4	A3	A2	A1	A0	R/$\overline{W}$
1	0	1	1	0	0	0	X

1

A6	A5	A4	A3	A2	A1	A0	R/$\overline{W}$
1	0	1	1	0	0	0	X

Purchase of TOSHIBA I^2C components conveys a license under the Philips I^2C Patent Rights to use these components in an I^2C system, provided that the system conforms to the I^2C Standard Specification as defined by Philips.

IIC BUS MAP

Sub	D7	D6	D5	D4	D3	D2	D1	D0
00H	INSEL		TVM3	TVM2	TVM1	TVM0	AUTODET	
	Select input signal 00:CVS (Composite Signal) 01:Y/C (Y/C Sep. Signal) 10:YCbCr (Component signal) 11:4fsc Data (Digital Signal)		Select FSC 0 :3.58MHz 1 :4.43MHz 0000 :NT358 0001 :don't use 0010 :PAL-M 0011 :don't use	Select FV 0 :60Hz 1 :50Hz 0100 :NT50 0101 :don't use 0110 :PAL-N 0111 :don't use	Select PAL 0 :Not PAL 1 :PAL 1000 :NT443 1001 :SEC60 1010 :PAL60 1011 :don't use	Select SECAM 0 :Not SECAM 1 :SECAM 1100 :don't use 1101 :SECAM 1110 :PAL 1111 :don't use	Set detection mode for Video System 00:Manual (00h-D5-D2) 01:European 10:South America 11:Full multi	
INIT:03H								
01H	3D DET Preset mode		YCS Mode YCS mode		FORMATO Output format	OUTBITS	HIZMODE Output control	ADPWD

Sub	D7	D6	D5	D4	D3	D2	D1	D0
10H	ACMSLP		ACSSLP		AYMSLP		AYSSLP	
	C slope at 1F (motion scene)		C slope at 1F (still picture scene)		Y slope at 1F (motion scene)		Y slope at 1F (still picture scene)	
INIT:5DH	00 :x1/2 ～ 11 :∞		00 :x1/2 ～ 11 :∞		00 :x1/2 ～ 11 :∞		00 :x1/2 ～ 11 :∞	
11H	ACMESET		ACMFSET		ACSESET		ACSFSET	
	C offset at 1F(edge, motion)		C offset at 1F (flat, motion)		C offset at 1F (edge, still)		C offset at 1F (flat, still)	
INIT:AAH	00 :still pixel～11 :motion pixel		00 :still pixel～11 :motion pixel		00 :still pixel～11 :motion pixel		00 :still pixel～11 :motion pixel	
12H	AYMESET		AYMFSET		AYSESET		AYSFSET	
	Y offset at 1F(edge, motion)		Y offset at 1F (flat, motion)		Y offset at 1F (edge, still)		Y offset at 1F (flat, still)	
INIT:AAH	00 :still pixel～11 :motion pixel		00 :still pixel～11 :motion pixel		00 :still pixel～11 :motion pixel		00 :still pixel～11 :motion pixel	
13H	BCMSLP		BCSSLP		BYMSLP		BYSSLP	
	C slope at 2F (motion scene)		C slope at 2F (still picture scene)		Y slope at 2F (motion scene)		Y slope at 2F (still picture scene)	
	00 :x1/2 ～ 11 :∞		00 :x1/2 ～ 11 :∞		00 :x1/2 ～ 11 :∞		00 :x1/2 ～ 11 :∞	
INIT:49H					〔YCSﾓｰﾄﾞのみ有効〕		〔YCSﾓｰﾄﾞのみ有効〕	
14H	BCMESET		BCMFSET		BCSESET		BCSFSET	
	C offset at 2F(edge, motion)		C offset at 2F (flat, motion)		C offset at 2F (edge, still)		C offset at 2F (flat, still)	
INIT:51H	00 :still pixel～11 :motion pixel		00 :still pixel～11 :motion pixel		00 :still pixel～11 :motion pixel		00 :still pixel～11 :motion pixel	
15H	BYMESET		BYMFSET		BYSESET		BYSFSET	
	Y offset at 2F(edge, motion)		Y offset at 2F (flat, motion)		Y offset at 2F (edge, still)		Y offset at 2F (flat, still)	
	00 :still pixel～11 :motion pixel		00 :still pixel～11 :motion pixel		00 :still pixel～11 :motion pixel		00 :still pixel～11 :motion pixel	
INIT:F5H								
16H	BCMUP	CECMP			CSCMP			
	C 2F Motion detection	The reference level for C edge detection			The reference level for C signal detection			
	0 :ON	000 :small ～ 111 :large			0000 :small ～ 1111 :large			
INIT:C3H	1 :OFF				〔for NR mode〕			
17H	F1HER		F1VER		MREF			
	Level for Y horizontal edge		Level for Y vertical edge		The reference level for scene detection			
	00 :OFF 10 :3 IRE		00 :OFF 10 :5 IRE		0000 :small ～ 1111 :large			
INIT:A4H	01 :6 IRE 11 :1.5IRE		01 :12 IRE 11 :2 IRE					
18H	CDEYE		YDEYE		MDS			3DSTD
	Reference level for scene det. C		Reference level for scene det. Y		Forced det.			Forced det.
	00 : 8% 10 :24%		00 : 8% 10 :24%		0 :normal	Fixed to [0]	Fixed to [0]	0 :normal
INIT:10H	01 :16% 11 :32%		01 :16% 11 :32%		1 :still			1 :std sig.
19H	2ASS	2ASEL	2ALEV		2ASSCM			CROS
	2F motion det. Correction	2F motion det. Select	2F motion det. judgment level		2F motion det. of C motion			Reduce Cross color
	0 :OFF	0:Y	000:OFF		00:motion pixel ～ 11:still pixel			0:ON
INIT:BEH	1 :ON	1:C	001:motion pixel ～ 111:still pixel					1:OFF
1AH	CHLPF	YDCLOFF	YDNRW	CDNRW	YDCMP[3:0]			
	Band width NR		Sensitivity Y Non correlation	Sensitivity C Non correlation	The reference level Y motion detection for 〔NR〕			
	0: wide	0 :OFF	0 :large	0 :large	0000:motion ～ 1111:still 〔1000〕			
INIT:08H	1: narrow	1 :Non-linear	1 :small	1 :small				
1BH	HDAMP1		HD GAIN1					
	Time constant 1 for H PLL		Loop gain 1 for H PLL					
INIT:89H	000 :large ～ 111 :small		00000 :small ～ 11111 :large					
1CH	HDAMP2		HDGAIN2					
	Time constant 2 for H PLL		Loop gain 2 for H PLL					
INIT:88H	000 :large ～ 111 :small		00000 :small ～ 11111 :large					
1DH	HDAMP3		HDGAIN3					
	Time constant 3 for H PLL		Loop gain 3 for H PLL					
INIT:A2H	000 :large ～ 111 :small		00000 :small ～ 11111 :large					
1EH	SHCTRL						MUTE	C MUTE
	H Reference						Mute	Chroma mute
	100000 :-4.74μs ～ 000000 :±0μs ～ 011111 :+4.46μs						0 :OFF	0 :OFF
INIT:00H							1 :ON	1 :ON
1FH	DOT DIST		COMB+	1LINE DOT	BCFOFF	CGAIN		
	Reduce H dots				BSRC filter	Ytrap performance for SECAM		
	00 :OFF 10 :x0.17		0 :OFF	0:ON	0: ON	000 :OFF ～ 111 :×0.875 (INT:110)		
INIT:FEH	01 :x0.16 11 :x0.18		1 :ON	1:OFF	1:OFF			

Sub	D7	D6	D5	D4	D3	D2	D1	D0
20H	ID1DLY				CCDSBH			
	The start timing of ID1 data slice				CCD start bit (H pulse period)			
INIT:8BH	0000 :Falling edge of H + 1. 48μs ～ 800ns unit)				1111:30CK～0000:0CK (*CK=74ns)			
21H		8OUTLSB					FIV	FON
	Fixed [0]	0] :Normal 1] :ON	Fixed [1]	Fixed [0]	Fixed [1]	Fixed [1]	Field for CCD slice 0:EVEN 1:ODD	CCD slice action 0:both field 1:FIV
INIT:80H								
22H	EN_NOISEH_S			EN_NOISEH_W			SSMSB	AUTO
	The horizontal start timing of S/N detection 000 :35.7uS ～ 100 :+40.5uS ～ 111 :44uS			The horizontal width of S/N detection 000 :10.2uS ～ 100 :14.9uS ～ 111 :18.5uS			Fixed to[1]	CCD slice 0:Auto 1:manual
INIT:90H	(1step: 32/27MHz)			(1step: 32/27MHz)				
23H	EN_NOISEV_S			EN_NOISEV_W		CLP	BYFOFF	BLMT
	Adjustment for S/N detection start line (Ex. NTSC mode) 2Fh(D3)=0, 000 :12th line～111 :18th line			S/N detection line number 00 :1H、01 :2H、10 :3H、11 :4H		16LSB limit (output) 0:OFF	BSRY filter 0:ON	V sepa. Limit 0: 1/8
INIT:0AH	2Fh(D3)=1, 000 :7th line～111 :13th line					1:ON	1:OFF	1: 1/16
24H	HDPH				VDPH			
	Adjustment Horizontal phase				Adjustment vertical phase			
INIT:00H	1000 :-1.185uS ～ 0000 :0uS ～ 0111 :+1.04uS				0000 :0H ～ 1111 :+15H			
25H	VPHS			CADSWREV	HDST		SELCK	
	VDOUT adjustment (601 mode) 110:384w 011:192w 000:0w 111:don't use 100:256w 001:64w 101:320w 010:128w			Cb/Cr Input 0 :Pin92=Cr-IN, Pin94=Cb-IN 1 :Pin92=Cb-IN, Pin94=Cr-IN	HDOUT adjustment (601) (See p.23)		CKOUT frequency 10:TEST 00:13.5MHz 11:13.5MHz 01::27MHz	
INIT:03H	64W=64/27MHz=2.4uS							
26H	PHPOLE	PVPOLE	PFPOLE	THRHV	INVCK	SEL_BLK	YOLEVEL	HHKIL
	HDOUT polarity 0: positive	VDOUT polarity 0:positive	Field Polarity 0:positive	H,V-OUT through 0:656	CKOUT Polarity 0:positive	VBLK 0:fixed value	Y Output Level Select 0:x1.7	Half H killer 0 :OFF
INIT:18H	1:negative	1:negative	1:negative	1:through(601)	1:negative	1:through	1:x1.0	1 :ON
27H	EN_PIXH_S				EN_PIXH_W			
	Adjustment horizontal signal processing (start phase)				Adjustment horizontal signal processing (period)			
INIT:00H	1000 :-1.185μs ～ 0000 :center ～ 0111 :+1.04μs				1000 :-1.185μs ～ 0000 :center～ 0111 :+1.04μs			
28H	EN_PIXV_S				EN_PIXV_A	COMB KILL		
	Adjustment vertical signal processing (start phase) 0000 :line 10 ～ 1111 :line 25				0 :Manual 1 :Auto	000 :OFF 001 :1～21H 010 :1～22H	011 :1～23H 100 :1～24H 101 :1～25H	110 :1～26H 111 :Auto (60:22H,50:23H)
INIT:07H								
29H	BFP_S						SEL_RDATA	
	Adjustment burst gate pulse start phase				[0] Fix		Select read data (Reference the next page)	
INIT:00H	0000 :±0 ～ 0111 :+4.44μs(4/13.5M step)							
2AH	HBLK_S				HBLK_W			
	Adjustment HBLK start phase				Adjustment HBLK width			
INIT:00H	1000 :-2.37μs ～ 0000 :±0 ～ 0111 :+2.07μs				1000 :-2.37μs ～ 0000 :±0 ～ 0111 :+2.07μs			
2BH	FHST_S				FVST_S			
	Adjustment write timing for internal DRAM (horizontal)				Adjustment write timing for internal DRAM (vertical)			
INIT:00H	1000 :-2.37μs ～ 0000 :±0 ～ 0111 :+2.07μs				1000 :-8H ～ 0000 :center ～ 0111 :+7H			
2CH	EXTCLP				SEL77	ACKDET	IIRFIL	
	Adjustment horizon position fine tuning for exterior clamp (6.75MHz unit、Width 2.2us Fix) After input sync edge about +0.5μs ～ about +3μs				Pin77 Output change 0:ODD/EVEN	Detection method change 0:Level detection	Cb/Cr output filter selection 00:Strong ～ 10:weak	
INIT:B2H	1000 :+0.5μs ～ 0111 :+3μs				1:Clamp pulse	1:Gain detection	11:OFF	
2DH	GCSFT							FBCLAMP
	GC Input DC shift 000000: 0、1000000:-128lsb ～ 0111111:+126lsb							F/B CLAMP 0:Auto 1:ON
INIT:01H								
2EH	HGCON12				HGCON21			
	Threshold from phase difference big to middle. 0000:OFF ～ 1111:High				Threshold from phase difference middle to big. 0000:OFF ～ 1111:High			
INIT:48H								
2FH	RBALT	RBCHG	YADFILON		NOISESEL	NOISEL	THRH_VD	
	Fixed [0]	Fixed [0]	ADC Output 13.5M Trap 0:OFF 1:ON Effective only at the time of a CVBS input	Fixed [1]	The line select for S/N detection (See p.24)	S/N detection Line 0 : CVBS/Y 1 : digital input	VD out phase (It is available when H-V is Non-standard) 0:standard 1:V-sep phase	Fixed [1]
INIT:00H								

READ MODE

07 | 00	DET50 Field frequency 0：60Hz 1：50Hz	NOSIG Sig.nal Det. 0：signal 1：no signal	NOVP V-Sync Det. 0：V det. 1：nonV	CFIELD Field 0：ODD 1：EVEN	UNLOCK H-PLL 0：un-locked 1：locked	H/VSTD H-V std 0:std. 1:non-std.	CRI3DET Fixed to [0]	 Fixed to [0]
0F | 08	DET443 4.43Det. 0:non 1:4.43	PALDET PAL Det. 0:not PAL 1:PAL	SECAMDET SECAM Det. 0:not SECAM 1:SECAM	SEL_FSC fsc detection 00:3.579545M 01:3.575611M 10:3.582056M 11:4.43M		CKILL Killer Det. 0:color 1:whit & black	FSCSTD fsc std Det. 0:std 1:non-std	FSCLOCK fsc lock 0:un-locked 1:lock
17 | 10	SNDET7	SNDET6	SNDET5	SNDET4	SNDET3	SNDET2	SNDET1	SNDET0
	S/N detection 00000000：strong signal → 11111111：Weak signal（MSB：SNDET7）							
1F | 18	0 Fixed to [0]	CFIELD Field 0：ODD 1：EVEN	SBDET CCD SB Det. 0:NG 1:OK	CRI3DET CCD CRI Det. 0:under 3ck 1:over 3ck	CRIN3	CRIN2 Number of CRI	CRIN1 (MSB)-----((LSB)	CRIN0
27 | 20	TSLV7 CCD Slice Level (MSB)	TSLV6	TSLV5	TSLV4	TSLV3	TSLV2	TSLV1	TSLV0 CCD Slice Level (LSB)
2F | 28	CCDD Character 1 CCD data LSB							CCD data
37 | 30	CCDD Character 2 CCD data							CCD data MSB
3F | 38	IICR ID1[0] Reference Signal Detection 0:OK 1:NG	IICR ID1[1] CRCチェック 0:OK 1:NG	IICR ID1[2] ID1 bit0 (WORD0)	IICR ID1[3] ID1 bit2 (WORD0)	IICR ID1[4] ID1 bit3 (WORD1)	IICR ID1[5] ID1 bit4 (WORD1)	IICR ID1[6] ID1bit5 (WORD1)	IICR ID1[7] ID1 bit6 (WORD1)
47 | 40	IICR ID1[8] ID1 bit7 (WORD2)	IICR ID1[9] ID1 bit8 (WORD2)	IICR ID1[10] ID1 bit9 (WORD2)	IICR ID1[11] ID1 bit10 (WORD2)	IICR ID1[12] ID1 bit11 (WORD2)	IICR ID1[13] ID1 bit12 (WORD2)	IICR ID1[14] ID1 bit13 (WORD2)	IICR ID1[15] ID1 bit14 (WORD2)
4F | 48	IICR ID1[16] ID1 bit15 (CRC code)	IICR ID1[17] ID1 bit16 (CRC code)	IICR ID1[18] ID1 bit17 (CRC code)	IICR ID1[19] ID1 bit18 (CRC code)	IICR ID1[20] ID1 bit19 (CRC code)	IICR ID1[21] ID1 bit20 (CRC code)	IICR ID1[22] Fixed to[0]	IICR ID1[23] Field det. 0:line 20 1:line 283
57 | 50	IICR ID1[24] ID1 Slice level MSB［7］	IICR ID1[25] ID1 Slice level	IICR ID1[26] ID1 Slice level	IICR ID1[27] ID1 Slice level	IICR ID1[28] ID1 Slice level	IICR ID1[29] ID1 Slice level	IICR ID1[30] ID1 Slice level	IICR ID1[31] ID1 Slice level LSB［0］

Select Read Data（29H :D1,D0）

The initial of Read Mode is “00”.

SEL_RDATA	1byte	2byte	3byte	4byte	5byte	6byte	7byte	8byte	9bite	10byte	11byte
00(Initial)	D1	D0	N0	C3	C2	C1	C0	I3	I2	I1	I0
01	D1	D0	C3	C2	C1	C0	N0	I3	I2	I1	I0
10	D1	D0	I3	I2	I1	I0	N0	C3	C2	C1	C0
11	I3	I2	I1	I0	D1	D0	N0	C3	C2	C1	C0

The explanation for IIC Bus

*Sub address 00h(D7-D6), 01h(D0) ADC power save mode

It can save the power automatically depending on the kind of input signal.

When it is not use the ADC, it can stop working ADC.

ADC Control 1 〔initial:00〕

Sub 00h D7 D6	Input signal	Y-ADC	C-ADC
0 0	CVBS	Normal	**Power save**
0 1	Y/C	Normal	Normal
1 0	Component	Normal	Normal
1 1	Digital	**Power save**	**Power save**

ADC Control 2 〔initial:1〕

Sub 01h D0	Input signal	Y-ADC	C-ADC
0	It does not depend on the input signal.	**Power down**	**Power down**
1		Normal	Normal

*Sub address 01h(D7-D6) 3D DET

It can switch preset mode for motion detection.

00: Preset mode for 3D YC separation

01: Preset mode for 3D NR

10: 3 line comb mode (NR off)

11: manual mode (It is available sub address 10h – 1Ah)

*Sub address 01H(D5-D4) YC separation mode

YC separation mode 〔initial:00〕

Sub 01h D5 D4	3.58M NTSC system	SECAM system	Other system
00	3DYCS	BPF YCS + 3DNR	3Line YCS + 3DNR
01	3Line YCS + 3DNR	BPF YCS + 3DNR	3Line YCS + 3DNR
10	BPF YCS + 3DNR	BPF YCS + 3DNR	BPF YCS + 3DNR
11	3Line YCS + 3DNR	BPF YCS + 3DNR	3Line YCS + 3DNR

- 3DYCS: 3D YC separation
- 3Line YCS: 3 line YC separation
- BPF YCS: Band Pass Filter YC separation
- 3DNR: 3D Noise Reduction

*Sub address 16h(D7) BCMUP

It can shift to motion seen for 2F motion detection of chroma signal.

If BCMUP is on, it can decrease a dot noise for continuous color change.

It must be attentive to increase a cross color noise when 2F motion detection for chroma is nearly motion.

*Sub address 19h 2F correction

It can control a phenomenon which the picture is in spite of still, it is treated as motion seen and appeared cross color noise.

19h(D7) 0:2F correction off 1:2F correction on

19h(D6) select a judgment standard signal

0:Working as base on motion detection result for 2F Y

1:Working as base on motion detection result for 2F C

19h(D5-D3) Setting a judgment level for working this function

000:off (same D7=0)

001:It is little effect

:

:

111:It is much effect

19h(D2) Setting motion detection for 2F correction

00: Moving picture direction

:

11: Still picture direction

Sub address 19h(D0) CROS

In case of moving picture for high frequency of Y signal, it can reduce a cross color noise.

*Sub address 1Ah Motion detection for 3DNR
1Ah(D7) Select a band width for NR working
0:Wide band (Recommended)
1:Narrow band

1Ah(D6)
When the picture is judged no color, it can control CNR motion detection for decreasing cross color noise.
0:motion detection for CNR is invalid.
1:Using still picture direction parameter

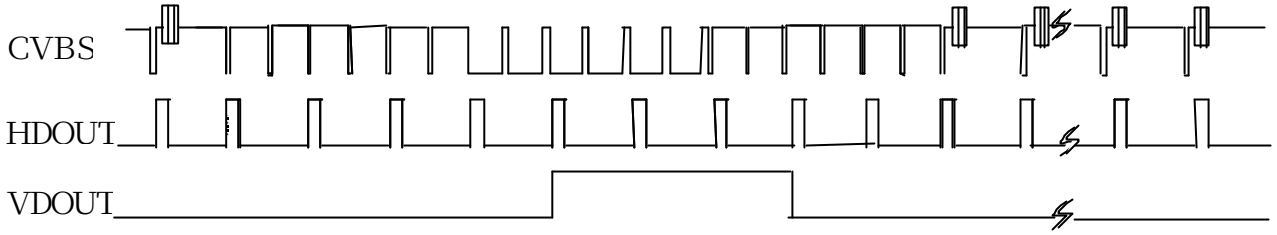
1Ah(D5) Setting non-correlation detection level for motion detection of Y
0:standard
1:two times of standard

1Ah(D4) Setting non-correlation detection level for motion detection of C
0:standard
1:two times of standard

1Ah(D3-D0) Setting Y signal moving amount judgment standard for NR
0000: Moving picture direction (There is little effect of decreasing cross color noise.)
:
1111: Still picture direction (There is many effect of decreasing cross color noise.)

*Sub address 1Fh(D5) COMB+
It has an effect as below for PAL system.
When the horizontal lines of the front and the rear have color and edge element, and the horizontal line of center has no color, it drops Y signal level for calculated result. Therefore it occurs dots of black in spite of white and gray picture. When COMB+ is on, it can decrease this noise.

*Sub address 24h Regarding digital output
24h(D7-D4) Setting horizontal phase for HDOUT
When sync signal is the same timing as HDOUT, the difference phase is 0us.
24h(D3-D0) Setting vertical phase for VDOUT
When vertical phase is 0H, timing diagram is as below.
This is available for H,V-OUT through mode. (26h:D4=1)



*Sub address 25h(D7-D5) VPHS: Setting VDOUT phase
When H,V-OUT through mode is on, it can shift VDOUT phase to horizontal direction. (2.4us step)

*Sub address 25h(D3-D2) HDST: Setting HDOUT phase
When H,V-OUT through mode is on, it can shift HDOUT phase.
It can delay HDOUT pulse from EAV based on standard.

Regarding 525 lines system
HDOUT phase (Default)
It is 32W from first point of EAV. (1W=1/27MHz)
HD width is about 4.73us. (128ck 1ck=1/27MHz)
00:32W(default) , 01:+4ck , 10:+8ck , 11:+16ck

Regarding 625 lines system
HDOUT phase (Default)
It is 24W from first point of EAV. (1W=1/27MHz)
HD width is about 4.73us. (128ck 1ck=1/27MHz)
00:24W(default) , 01:+4ck , 10:+8ck , 11:+16ck

*Sub address 26h(D5) PFPOLE,(D2) SEL_BLK
26h(D5) Setting field polarity
When the polarity is positive, 1st field is low.
26h(D2) the disposal of blanking period
0:It is masked the signal under pedestal level.
1:Through

*Sub address 2Fh(D5) 13.5M Trap

It can decrease the interference with 13.5MHz regarding to fh frequency and 14.3MHz regarding to fsc frequency.

0:OFF

1:ON (In this case, it needs to revise high frequency as below.)

(The relation resister)

Sub address 1Eh(D7-D2) Horizontal reference

When input signal is CVBS, it needs to shift 1 step. (000000→111111)

Sub address 04h(D1) Sharpness fo

Sub address 05h(D7-D6) Sharpness gain

If sharpness fo = 4.2MHz and sharpness gain = x1/8, the frequency characteristic is the same as trap-off.

*Sub address 22h、Sub23h、2Fh(D3) Regarding noise detection

22h(D7-D5) Horizontal start phase from under direction edge of H sync

22h(D4-D2) Horizontal width

23h(D7-D5) Vertical start phase

23h(D4-D2) Vertical line number select

【1-A】**When sub address 2Fh (D3)=0, it is the start line number.**

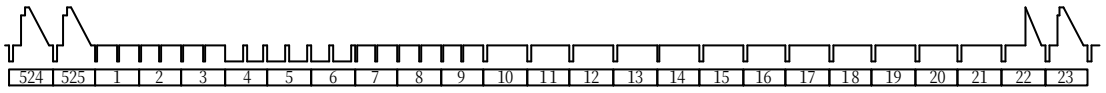
Sub address 23h (D7-D5)	ODD FIELD		EVEN FIELD	
	NTSC (Line number)	PAL (Line number)	NTSC (Line number)	PAL (Line number)
000	12	9	274	321
001	Non detection	10	275	322
010	13	11	276	323
011	14	12	277	324
100	15	13	278	325
101	16	14	279	326
110	17	15	280	327
111	18	16	281	328

【1-B】**When sub address 2Fh (D3)=1, it is the start line number.**

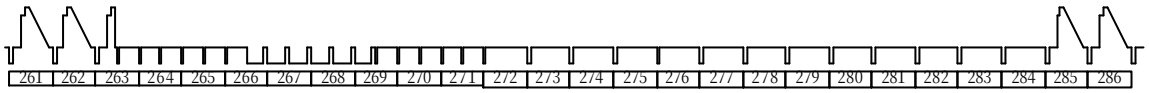
Sub address 23h (D7-D5)	ODD FIELD		EVEN FIELD	
	NTSC (Line number)	PAL (Line number)	NTSC (Line number)	PAL (Line number)
000	7	4	269	316
001	8	5	270	317
010	9	6	271	318
011	10	7	272	319
100	11	8	273	320
101	12	9	274	321
110	Non detection	10	275	322
111	13	11	276	323

【Fig4】The line number for vertical period

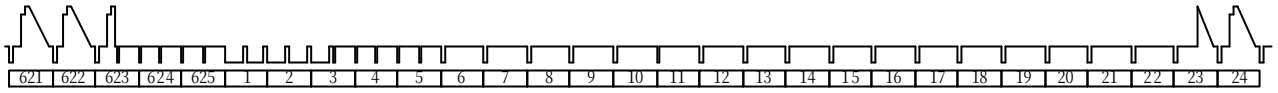
NTSC (525Line/60Hz) 1st Field (odd)



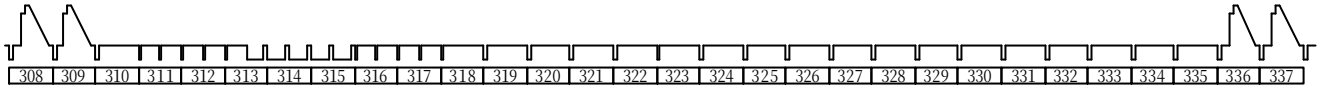
NTSC (525Line/60Hz) 2nd Field (even)



PAL (625Line/50Hz) 1st Field (odd)



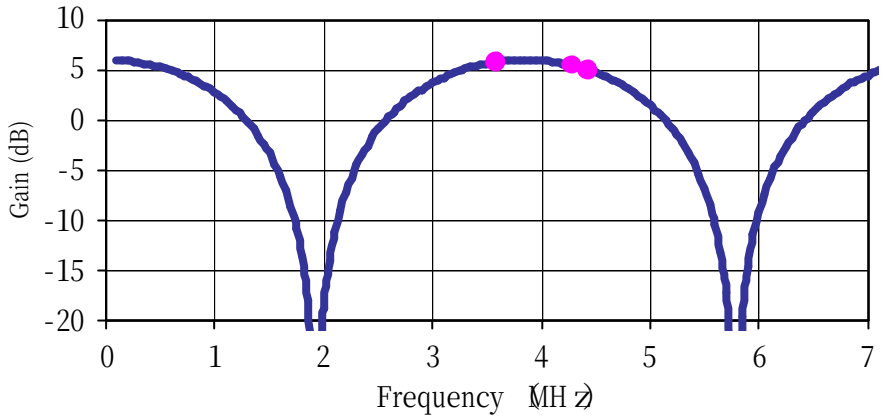
PAL (625Line/50Hz) 2nd Field (even)



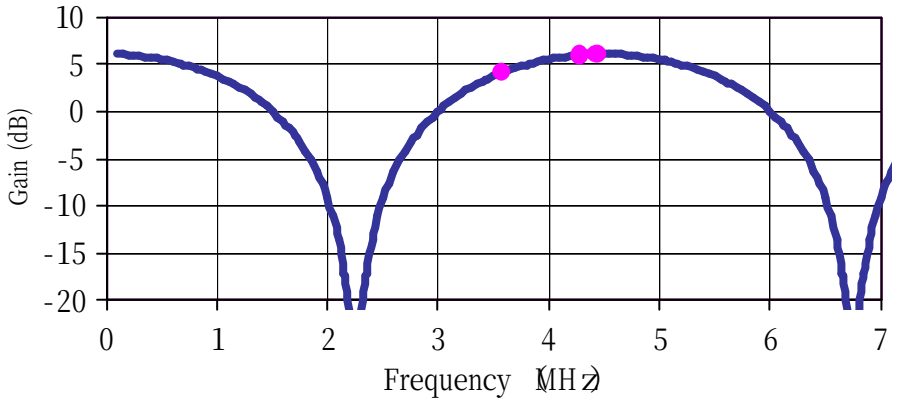
*Sub address 2Fh(D2) Signal select for noise detection

【Fig.5】

TC90A92AFG the band limit characteristic
for color decoder (NTSC)
(Marker : 3.58M, 4.286M, 4.43MHz)



TC90A92AFG the band limit characteristic
for color decoder (PAL)
(Marker : 3.58M, 4.286M, 4.43MHz)



*Sub address 2Fh(D1) VD out phase select when H-V is non-standard and H,V-OUT is through mode.
0: standard phase (VD output after counted standard line number)
1: VD output as base on result of V-sep

*Sub address 21h(D6) 8OUTLSB
It can reduce quantization noise when 10 bit signal convert to 8 bit at output stage.
This effect changes in GND condition.
When output signal is 10 bit, it needs to set to normal mode.
0: Normal
1: ON (Quantization noise reduction is active.)

MAXIMUN RATINGS (Vss=0V, Ta=25°C)

Each item of the maximum rating shows the marginal value of this product. Since a product is sometimes damaged when rating is exceeded also one item or for a moment again, be sure to use it within rating.

CHARACTERISTIC	SYNBOL	RATING	UNIT
Power Supply Voltage1 (1.5V System)	VDD1	-0.3 ～ VSS+2.0	V
Power Supply Voltage2 (2.5V System)	VDD2	-0.3 ～ VSS+3.5	V
Power Supply Voltage3 (3.3V System)	VDD3	-0.3 ～ VSS+3.9	V
Input Voltage	VIN	-0.3 ～ VDDIO +0.3	V
	SDA/SCL(Note1)	-0.3 ～ VSS + 5.5	V
	A IN	-0.3 ～ VDDAD	V
Potential difference between power supply terminals (1.5V System)	VDG1 (Note2)	0.3	V
Potential difference between power supply terminals (2.5V System)	VDG2 (Note2)	0.3	V
Potential difference between power supply terminals (3.3V System)	VDG3 (Note2)	0.3	V
Potential difference between power supply terminals (1.5V System＞2.5V System)	VDG4 (Note2)	0.3	V
Potential difference between power supply terminals (2.5V System ＞3.3V System)	VDG5 (Note2)	0.3	V
Power Dissipation	PD(Note3)	1530	mW
Storage Temperature	Tstg	-40 ～ 125	°C

(Note1) SDA, SCL： 5V tolerance.

(Note2) 1.5V system power supply terminal is made into the same voltage, 2.5V system power supply terminal is made into the same voltage, and 3.3V system power supply terminal is made into the same voltage.
The maximum potential difference should not exceed rating for all power supply terminals then.

(Note3) Derated above Ta=25°C in the proportion of 15.3mW/°C.

Recommendation operation conditions (Vss=0V)

Cannot guarantee operation of TC90A92F, when the recommendation power supply voltage range (1.35V-1.65V, 2.3V-2.7V, 3.0V-3.6V) is exceeded.
Once, when it returns from the over range, it differs from a front condition.
When the memory block exceeds the range especially,
it is necessary to once bring down a power supply and to newly rise.

CHARACTERISTIC	Terminal No.	SYNBOL	MIN	TYP	MAX	UNIT
Supply Voltage for digital block	10,17,36,59,70	DVDD1-5	1.35	1.5	1.65	V
Supply Voltage for I/O block	24,42,64	VDDIO1-3	3.0	3.3	3.6	V
Supply Voltage for DRAM block	21,51	VDDRAM1	1.35	1.5	1.65	V
Supply Voltage for DRAM block	53	VDDRAM2	2.3	2.5	2.7	V
Supply Voltage for XO block	5	VDDXO	3.0	3.3	3.6	V
Supply Voltage for PLL block	1	VDDPLL	2.3	2.5	2.7	V
Supply Voltage for Analog block	86,91,96	VDDAD/VDDDA	2.3	2.5	2.7	V
Ambient operating temperature	-	Ta	-10	—	75	°C

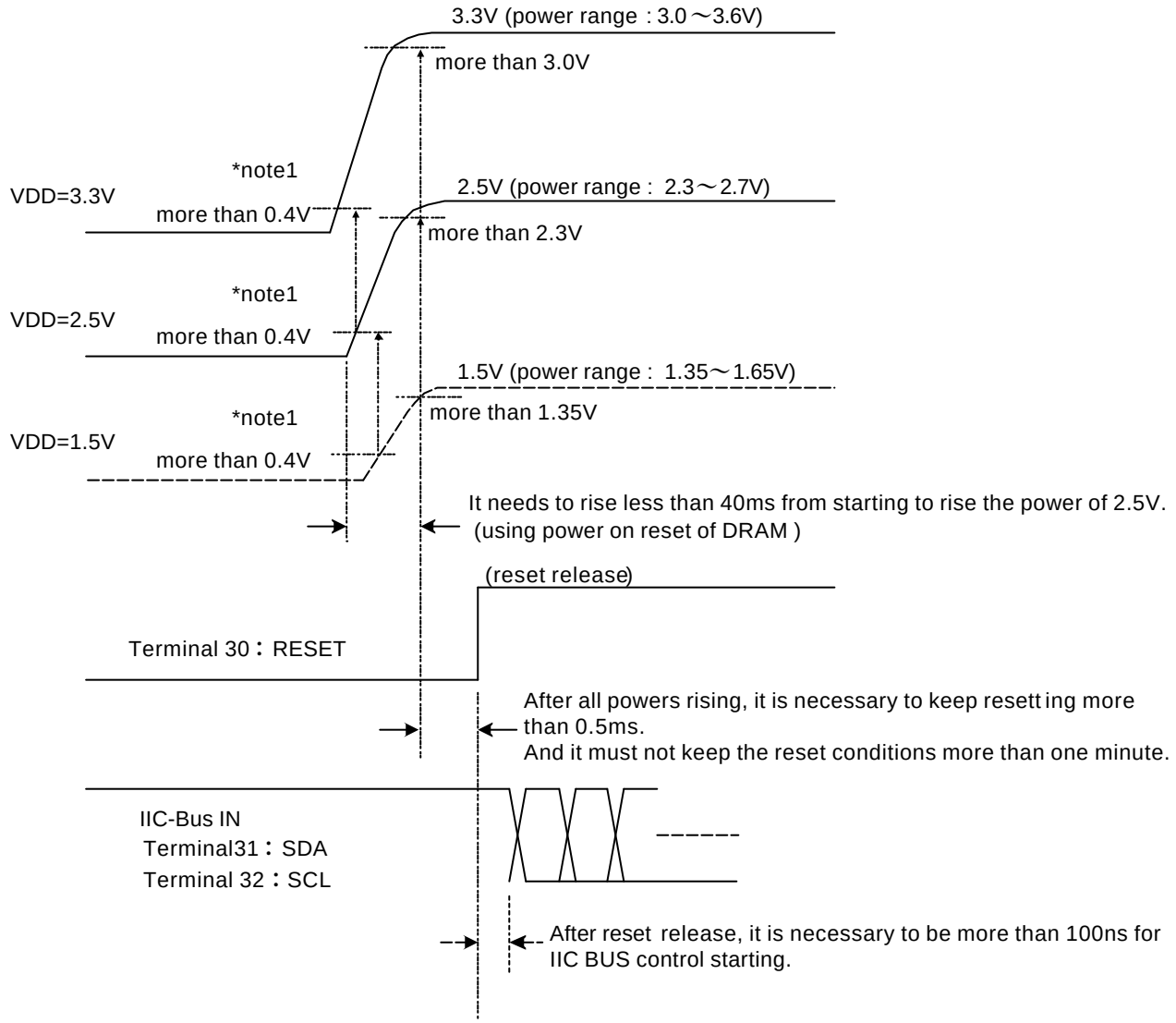
The condition of power (VDD=3.3V, 2.5V, 1.5V) rising and falling

(1)Power Supply rising

These contents are the important items which influence the reliability guarantee of the IC.

It is necessary to satisfy the following condition.

(1) Power rising condition



*note1

Such the power terminal are embedded the protective diode.

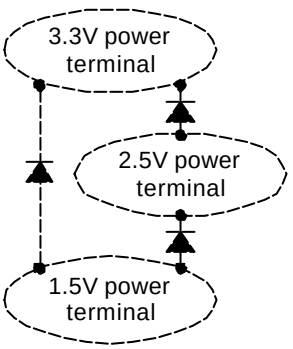
It must not send a penetration electric current.

Condition:

Power level of 3.3V line ≧Power level of 2.5V line ≧Power level of 1.5V line

When the power level of 1.5V line is more than 0.4V, 3.3V line and 2.5V line must reach the level of power more than 0.4V.

And when the power level of 2.5V line is more than 0.4V, 3.3V line must reach the level of power more than 0.4V.



(2) Power falling condition

It is necessary to fall the power of 1.5V line before 3.3V line and 2.5V line are fallen, and to fall the power of 2.5V line before 3.3V line is fallen.

It must not send a penetration electric current too.

ELECTRICAL CHARACTERRISTICS

(1) DC CHARACTERRISTICS

(Ta= -10～75℃,VDD1=1.50±0.15V,VDD2=2.50±0.2V,VDD3=3.30±0.3V)

ITEM	Terminal No.	Symbol	Min.	Typ.	Max.	Unit	Note
Power Supply Current	10,17,21,36,51,59,70	IDD1	30	42	55	mA	Sum total current of 1.5V system power supply terminal NTSC:Y/C IN, Color Bar Signal
	1,53,86,91,96	IDD2	60	75	95	mA	Sum total current of 2.5V system power supply terminal NTSC:Y/C IN, Color Bar Signal
	5,24,42,64	IDD3	10	25	40	mA	Sum total current of 3.3V system power supply terminal Changes with the loads of I/O.
Input Voltage	6,9,11,12,13,15,16, 18,19,22,23,25,26, 28,29,30,33,34,35, 37,40,41	VIH	VDDx0.8		VDD	V	I/O input terminal of 3.3V system VDD=VDD3
	31,32,38						I/O input terminal of 5.0V system VDD=5.25V
	6,9,11,12,13,15,16, 18,19,22,23,25,26, 28,29,30,33,34,35, 37,40,41	VIL	VSS		VDD3x0.2	V	I/O input terminal of 3.3V system
	31,32,38						I/O input terminal of 5.0V system
Input Current	6,9,11,12,13,15,16, 18,19,22,23,25,26, 28,29,30,33,34,35, 37,40,41	IIH	-10		10	μA	3 I/O input terminal of 3.3V system
	31,32,38						I/O input terminal of 5.0V system
	6,9,11,12,13,15,16, 18,19,22,23,25,26, 28,29,30,33,34,35, 37,40,41	IIL	-10		10	μA	I/O input terminal of 3.3V system
	31,32,38						I/O input terminal of 5.0V system
Output Voltage	43,44,46,47,48,49,54, 55,56,57,58,60,61,63, 65,66,68,69,71,72,74 75,76,77,78,79,80	VOH	VDD3-0.6		VDD3	V	I/O output terminal of 3.3V system Load of 4mA inflow
	43,44,46,47,48,49,54, 55,56,57,58,60,61,63, 65,66,68,69,71,72,74 75,76,77,78,79,80	VOL	VSS		0.4	V	I/O output terminal of 3.3V system Load of 4mA inflow
	31						I/O output terminal of 5.0V system Load of 4mA inflow

(2) AC CHARACTERRISTICS

(Ta=25℃,VDD1=1.50V,VDD2=2.50V,VDD3=3.30V)

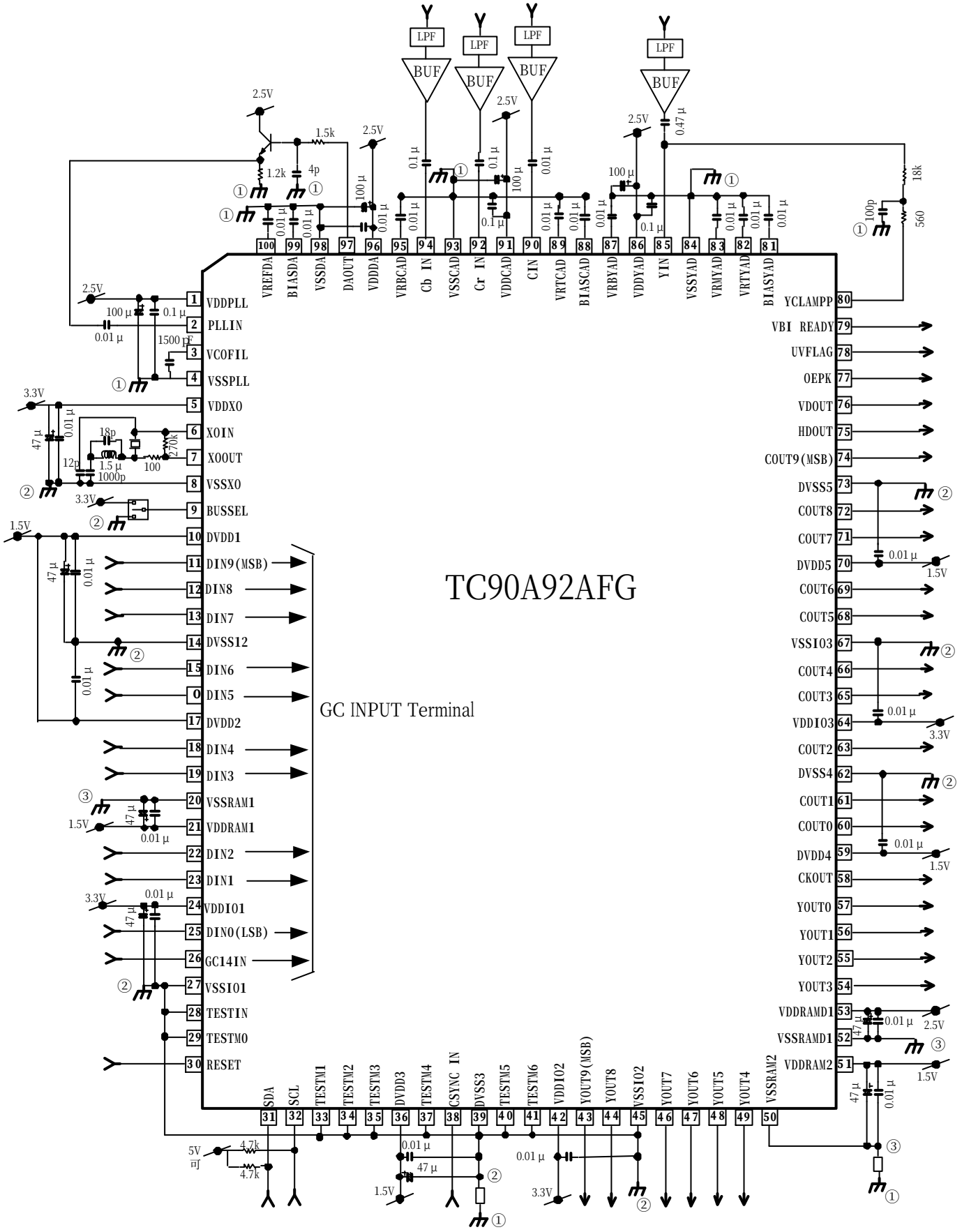
ITEM	Symbol	Min.	Typ.	Max.	Unit	Note
AD input level for Y	VYIN		0.7	0.8	Vp-p	White 100% Signal
AD input level for C	VCIN		0.5	0.8	Vp-p	Cb/Cr input
ADC differentiation error	DLEa		±4		LSB	
ADC integration error	ILEa		±4		LSB	
Output impedance	Zy	160	200	240	Ω	

(3) PLL CHARACTERRISTICS

(Ta=25℃,VDD1=1.50V,VDD2=2.50V,VDD3=3.30V)

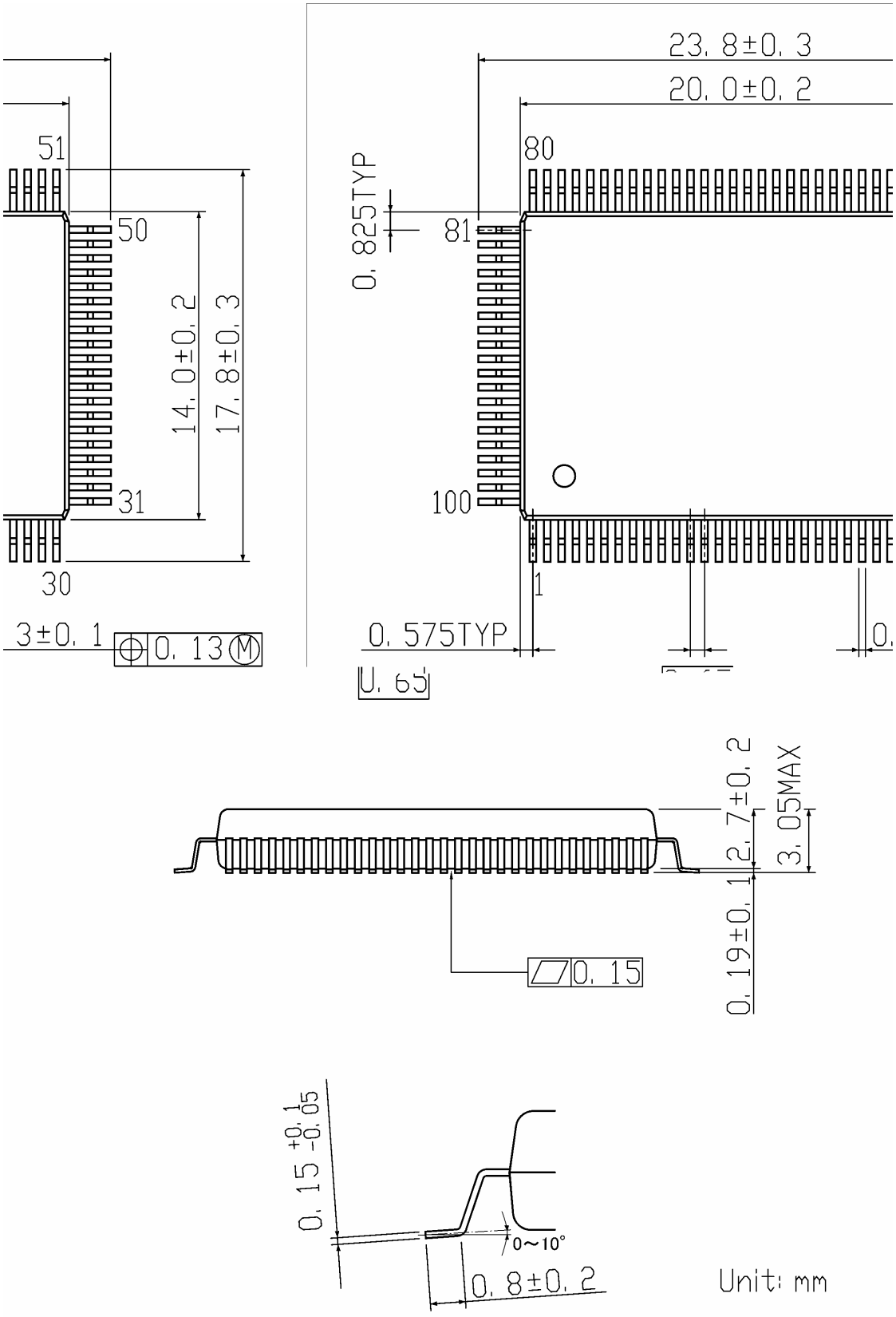
ITEM	Symbol	Min.	Typ.	Max.	Unit	Note
Drawing-in frequency range	ΔfckN	-50		50	kHz	Clock Amplitude:0.5Vp-p
Operation input amplitude	Vck	0.3	0.5	2.0	Vp-p	Standard clock frequency input

Application Circuit

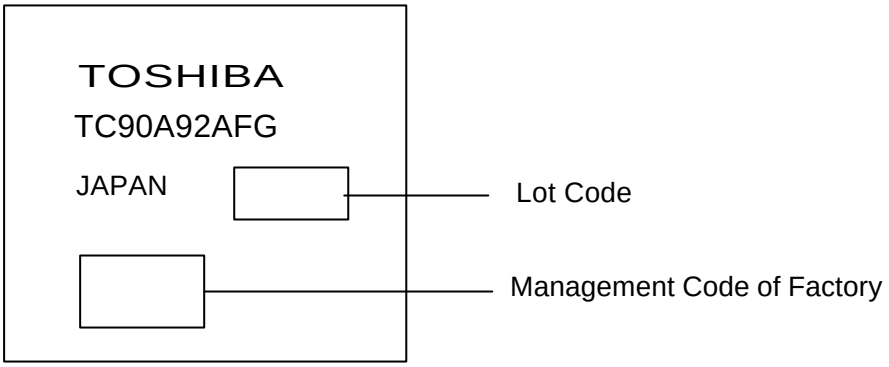


●PACKAGE DIMENSIONS

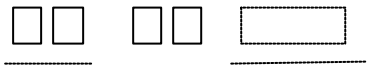
QFP100-P-1420-0.65Q



Marking



Explanation for lot code



Production management number

Weekly code

The first week of January is assigned the code number 01, the second week 02 etc. The last week of December is either 52 or 53. This is determined as follows.

Provided that the 1st January does not fall on a Friday or Saturday, the week which runs from the final Sunday of the old year to the first Saturday of the new year is designated as the first week of the new year [01]. If the 1st January falls on a Friday or Saturday, the week which runs from the final Sunday of the old year to the first Saturday of the new year is designated as the 53rd week of the preceding year [53].

The year of manufacture
(The last two digits for AD)

Mold material: Epoxy resin

Lead material: Copper base alloy

Lead surface treatment: Palladium plating

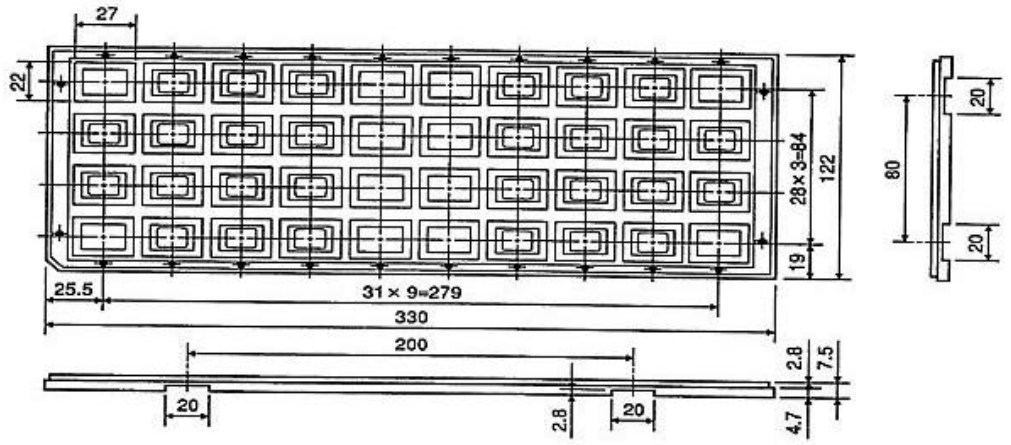
Country of origin: Japan

Works: TOSHIBA Ooita Works

Packing of QFP100-P-1420 Tray

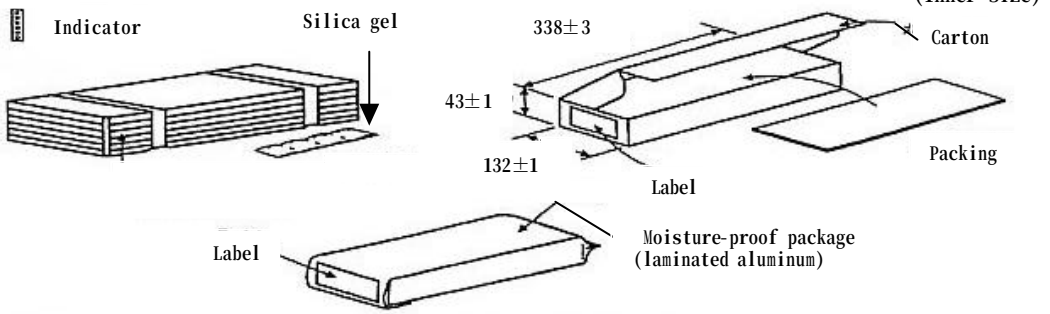
1.Device Holder

Unit: mm

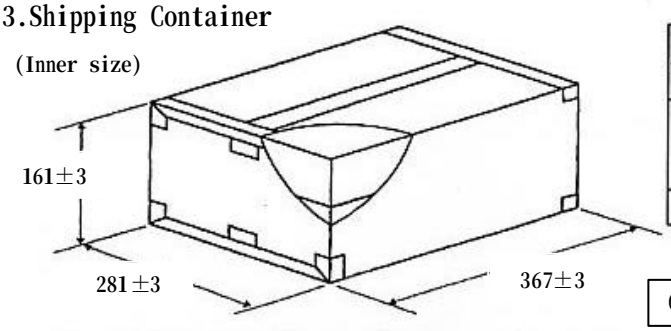


Package Code	Maximum Number of Packed Product
QFP100-P-1420-0.65	40 products/tray 200 products/carton 1200 products/container

2.Carton



3.Shipping Container



Label

TYPE			
ADD.C		Q'TY	PCS
NOTE			

Bar code

Outer size W:291mm L:377mm H:176mm